## IN THE CLAIMS

1. (original) A synchronous memory interface comprising:

data communication connections adapted to provide bi-directional data communication with an external communication bus;

data buffer coupled to the data communication connections, wherein the data buffer is adapted to manage the bi-directional data communication and buffer data that is input and/or output from the synchronous memory interface;

a write latch coupled to the data buffer, wherein the write latch is adapted to latch data written to the synchronous memory interface on the data communication connections separate from the data buffer; and

wherein the synchronous memory interface is adapted to receive a read operation and/or transmit read data while a write operation is executed from the write latch.

2. (original) The synchronous memory interface of claim 1, wherein the synchronous memory interface is adapted to receive a write operation command and latch it in the write latch during a wait period of a read operation.

3. (original) The synchronous memory interface of claim 2, wherein the wait period is a read command column address strobe (CAS) latency time period.

4. (original) The synchronous memory interface of claim 1, wherein the synchronous memory interface is adapted to receive a write operation command on the data communication connections and latch the write operation command in the write latch.

5. (original) The synchronous memory interface of claim 1, wherein the synchronous memory interface is adapted to receive a write operation command on a first clock cycle and latch it in the write latch and receive a read command on a second clock cycle, where the second clock cycle immediately follows the first.

6. (original) A method of reducing latency in a synchronous memory device comprising:

receiving write data on a first clock cycle;

storing the write data and executing a data write operation; and

executing a data read operation on a next clock cycle immediately following the first clock cycle.

7. (original) The method of claim 6, wherein the data write operation is executed on a first memory bank of the synchronous memory device and the data read operation is executed on a second memory bank.

8. (original) The method of claim 6, wherein the data write operation is executed on a first erase block of the synchronous memory device and the data read operation is executed on a second erase block.

9. (original) The method of claim 6, wherein receiving write data on a first clock cycle and storing the write data and executing a data write operation further comprises latching the write data in an internal write latch on the first clock cycle.

10. (original) The method of claim 6, wherein executing the data write operation comprises:

receiving a write command;

receiving a row address; and

receiving a column address, wherein the column address is received on the first clock cycle in synchronization with the write data.

11. (original) The method of claim 6, further comprises:

latching the write data in a write latch on the first clock cycle; and

performing a write operation during the next clock cycle to store the write data in the synchronous memory device.

12. (original) A method of command interleaving in a synchronous memory device comprising:

receiving a read command to initiate a read operation; and

receiving a write command sequence during a wait period of the read operation or concurrently with output of data from the read command.

13. (original) The method of claim 12, wherein the wait period is a read command column address strobe (CAS) latency time period.

14. (original) The method of claim 12, wherein the write command sequence comprises:
a load command register cycle used to initiate the write operation;
an active cycle used to define and activate a selected row of the memory array; and
a write cycle used to define a column of the memory array and provide write data on the external data connection.

15. (original) A method of operating a synchronous memory bus in a memory system, the method comprises:
providing a read command across a synchronous memory bus to a synchronous memory device to initiate a read operation;
providing a memory array address across the synchronous memory bus to the synchronous memory device on a first clock cycle of the synchronous memory bus to perform the read operation; and
providing a first command of a write command sequence across the synchronous memory bus to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation such that the write command is provided prior to or concurrently with providing output read data from the read operation on an external data connection of the synchronous memory device.

16. (original) The method of claim 15, wherein providing a write command across a synchronous memory bus to a synchronous memory device further comprises latching the write command in an internal write latch.

17. (original) The method of claim 15, wherein providing a write command across a synchronous memory bus to a synchronous memory device further comprises providing at least a load command register cycle.

18. (original) A method of operating a synchronous memory bus in a memory system, the method comprises:

providing a write command across a synchronous memory bus to a synchronous memory device to initiate a write operation;

providing write data across a synchronous memory bus to the synchronous memory device on a first clock cycle of the synchronous memory bus; and

providing a read command across the synchronous memory bus to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation.

19. (original) The method of claim 18, wherein providing a write command and write data across a synchronous memory bus to a synchronous memory device further comprises latching the write command and write data in an internal write latch.

20. (original) The method of claim 18, wherein providing a write command and write data across a synchronous memory bus to a synchronous memory device comprises:

providing a write command;

providing a row address; and

providing a column address, wherein the column address is provided on the first clock cycle in synchronization with the write data.

21. (currently amended) A method of operating a synchronous memory device comprising:

executing a write operation <u>from an internal write latch</u> on a first part of a memory array of the synchronous memory device while executing a read operation on a second part of the memory array.

22. (original) The method of claim 21, wherein the first and second part of the memory array further comprises a first and second memory bank.

23. (original) The method of claim 21, wherein the first and second part of the memory array further comprises a first and second erase block.

24. (currently amended) The method of claim 21, wherein executing a write operation from an internal write latch on a first part of a memory array further comprises executing a write operation from an internal write latch, where a synchronous memory interface of the synchronous memory receives a write operation command on a first clock cycle and latches it in the write latch and receives a read command on a second clock cycle, where the second clock cycle immediately follows the first.